ABSTRACT OF THE DISCLOSURE

In a method and apparatus for enabling fast clock phase locking in a phase-locked loop, a sampling clock generator generates sampling clock signals in response to an oscillator output of the phase-locked loop. A detector unit samples an input digital signal to the phase-locked loop at clock edges of the sampling clock signals to obtain multiple sampling points of the input digital signal, and compares logic levels of each temporally adjacent pair of the sampling points to detect presence of a logic level transition in the input digital signal. A selector unit is controlled by the detector unit to select one of the sampling clock signals, which has one of the clock edges thereof defining an interval that was detected to have occurrence of the logic level transition in the input digital signal, and which is subsequently provided to the phase-locked loop as an input phase-locking clock signal.